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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,967	12/21/2001	James Chow	01-S-078	7501

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EXAMINER	
PHU, PHUONG M	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,967	CHOW ET AL.	
	Examiner	Art Unit	
	Phuong Phu	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the Amendment filed on 10/20/05.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 6-14, 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al (6,538,486), previously cited.

-Regarding to claims 1 and 12, see figures 1 and 2, and col. 1, lines 10-40 and col. 2, line 18 to col. 3, line 40, Chen et al discloses a system (see figure 2) comprises:

a latch circuit (18) for sampling a differential data signal (V_{IN}) in response to a first strobe signal (being derived from (22));

an inverter element, the first strobe signal being an input to the delay element (see figure 2, the inverter element located at a trigger input of (20)) (note that the inverter element is

considered equivalent with the limitation "delay element" because the inverter element inherently delays its input signal to produce its output via the inverting process of the inverter; and in order to clarify the inherency of the delaying function of an inverter, see reference (5,945,862)), and

a strobe circuit (20) coupled to the latch circuit, the strobe circuit capturing the output of the latch circuit based on a second strobe signal (being derived from (22)) outputted from the inverter element (see figure 2).

-Regarding to claims 2 and 13, in Chen et al system, discloses that the latch circuit (see figure 1) produces a voltage change at output (V_{OUT}) that is inherently less than the voltage difference between a power supply voltage (Vc) that supplies the latch circuit and ground since, as shown in figure 1, the voltage difference is equal power supply voltage (Vc), and the output (V_{OUT}), as being derived from the supply voltage (Vc), is less than power supply voltage (Vc), namely less than the voltage difference.

-Regarding to claims 3 and 14, Chen et al discloses the latch circuit (18) (see figures 2 and 1)) is an analog latch circuit comprising analog devices (see figure 1) that latches or holds the differential data signal (V_{IN}, V^{-}_{IN}) in response to the first strobe signal (Clk, Clk^{-}) so as to produce a latched voltage (V_{OUT}, V^{-}_{OUT}) (see col. 1, lines 10-30) , and the strobe circuit (20) (see figures 2 and 1) samples and holds the latched voltage in order to determine a logic level of the differential data signal (see figure 1, and col. 1, lines 10-30).

-Regarding to claim 6, Chen et al discloses that the output of the latch circuit comprises a set of differential output nodes (9, 8) and the latch circuit includes load elements ((R,7), (R,6))

provided between a power supply input and the set of differential output nodes, each of the load elements including a transistor (7, 6) (see figure 1).

-Regarding to claims 7 and 16, Chen et al discloses that the latch circuit (see figure 1) includes: an input, an input branch (2) and a latch branch (5) connected in parallel between the input (A) and an output (to the input of I_0) ; and a bias current control transistor (including a transistor (receiving Clk) and (I_0)) coupled in series between the output and both the input branch and the latch branch (see figure 1).

-Regarding to claims 8 and 17, Chen et al discloses that the input branch of the latch circuit includes: a pair of differential input transistors (2) electrical coupled to the input; and a single strobe transistor (receiving Clk-) coupled in series between the pair of differential input transistors and the bias current control transistor (see figure 1).

-Regarding to claims 9 and 18, Chen et al discloses that the latch circuit receives only one bias voltage (Vc) for controlling an amount of current passing through the latch circuit (see figure 1).

-Regarding to claims 10 and 19, Chen et al discloses that a buffer (16) having an output coupled to the input of the latch circuit (18), the buffer receiving a differential input signal (see figure 2).

-Regarding to claims 11 and 20, Chen et al discloses that the differential input signal received by the buffer is composed of a single input data signal (V_{OUT}) and a reference voltage (V_{OUT}), being outputted from (14) (see figures 2 and 14).

Response to Arguments

3. Applicant's arguments filed on 10/20/05, with respect to the rejection under 35 USC 102 and 103, have been considered but are moot in view of the new ground(s) of rejection.

4. The previous objection to the Drawings has been withdrawn since the Drawings were amended and overcome the objection.

5. The previous rejection, under 35 USC 112, second paragraph, to claims 6-9 and 16-18 has been withdrawn since the corresponding claims were amended and overcome the rejection.

Conclusion

6. Reference 5,945,862 is additionally cited because they are pertinent to the claimed system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (6:30-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuong Phu
Primary Examiner
Art Unit 2631

Phuong Phu
PHUONG PHU
PRIMARY EXAMINER
Phuong Phu
12/19/05